VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination – 2018-19
M.Tech in Digital Electronics / Electronics (ELD)
Choice Based Credit System (CBCS)

I SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18ELD11	Advanced Engineering Mathematics	04	--	03	40	60	100	4
2	PCC	18ECS12	Advanced Digital Signal Processing	04	--	03	40	60	100	4
3	PCC	18EVE13	Advanced Embedded System	04	--	03	40	60	100	4
4	PCC	18ELD14	Digital Circuit and Logic Design	04	--	03	40	60	100	4
5	PCC	18EVE15	Digital VLSI Design	04	--	03	40	60	100	4
6	PCC	18ELDL16	Embedded Systems Lab	-	04	03	40	60	100	2
7	PCC	18RMI17	Research Methodology and IPR	02	--	03	40	60	100	2
			TOTAL	**22**	**04**	**21**	**280**	**420**	**700**	**24**

Note: PCC: Professional core.

Internship: All the students shall have to undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. A University examination will be conducted during III semester and prescribed credit shall be included in the III semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as failed and have to complete during subsequent University examination after satisfying the internship requirements.

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II SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18ELD21	Advanced Computer Architecture	04	--	03	40	60	100	4
2	PCC	18EVE22	Real Time Operating System	04	--	03	40	60	100	4
3	PCC	18ECS23	Error Control Coding	04	--	03	40	60	100	4
4	PEC	18XXX24X	Professional Elective 1	04	--	03	40	60	100	4
5	PEC	18XXX25X	Professional Elective 2	04	--	03	40	60	100	4
6	PCC	18ELDL26	Digital Circuits Simulation Lab	--	04	03	40	60	100	2
7	PCC	18ELD27	Technical Seminar	--	02	--	100	--	100	2
TOTAL				**20**	**06**	**18**	**340**	**360**	**700**	**24**

Note: PCC: Professional core, PEC: Professional Elective.

Professional Elective 1		**Professional Elective 2**	
Course Code under 18XXX24X	**Course title**	**Course Code under 18XXX25X**	**Course title**
18ECS241	Wireless Sensor Networks	18EIE251	Automotive Electronics
18EVE242	Nanoelectronics	18EVE252	SoC Design
18ECS243	Cryptography and Network Security	18ELD253	Micro Electro Mechanical Systems

Note:

1. Technical Seminar: CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide in any and a senior faculty of the department. Participation in seminar by all postgraduate students of the same and other semesters of the programme shall be mandatory.

The CIE marks awarded for Technical Seminar, shall be based on the evaluation of Seminar Report, Presentation skill and Question and Answer session in the ratio 50:25:25.

2. Internship: All the students shall have to undergo mandatory internship of 6 weeks during the vacation of I and II semesters and /or II and III semesters. A University examination will be conducted during III semester and prescribed credit shall be included in the III semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take-up/complete the internship shall be declared as failed and have to complete during subsequent University examination after satisfying the internship requirements.

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III SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks	Total Marks	
1	PCC	18ELD31	Synthesis and Optimization of Digital Circuits	04	--	03	40	60	100	4
2	PEC	18XXX32X	Professional Elective 3	04	--	03	40	60	100	4
3	PEC	18XXX33X	Professional Elective 4	04	--	03	40	60	100	4
4	Proj	18XXX34	Evaluation of Project phase -1	--	02	--	100	--	100	2
5	INT	18ELD35	Internship	(Completed during the intervening vacation of I and II semesters and /or II and III semesters.)		03	40	60	100	6
TOTAL				12	02	12	**260**	**240**	**500**	**20**

Note: PCC: Professional core, PEC: Professional Elective, Proj: Project, INT: Internship.

Professional Elective 3		**Professional Elective 4**	
Course Code under 18XXX32X	**Course title**	**Course Code under 18XXX33X**	**Course title**
18ECS321	Advances in Image Processing	18EVE331	VLSI Design for Signal Processing
18EVE322	CMOS RF Circuits Design	18ESP332	Pattern Recognition & Machine Learning
18ESP323	Communication System Design using DSP Algorithms	18ECS333	Internet of Things

Note:
1. Project Phase-1: Students in consultation with the guide/co-guide if any, shall pursue literature survey and complete the preliminary requirements of selected Project work. Each student shall prepare relevant introductory project document, and present a seminar.
CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide and a senior faculty of the department.The CIE marks awarded for project work phase -1, shall be based on the evaluation of Project Report, Project Presentation skill and Question and Answer session in the ratio 50:25:25.
SEE (University examination) shall be as per the University norms.
2. Internship: Those, who have not pursued /completed the internship shall be declared as failed and have to complete during subsequent University examinations after satisfying the internship requirements.
Internship SEE (University examination) shall be as per the University norms.

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IV SEMESTER

Sl. No	Course	Course Code	Course Title	Teaching Hours /Week		Examination				Credits
				Theory	Practical/ Field work/ Assignment	Duration in hours	CIE Marks	SEE Marks Viva voce	Total Marks	
1	Proj	18ELD41	Project work phase -2	--	04	03	40	60	100	20
			TOTAL	--	**04**	**03**	**40**	**60**	**100**	**20**

Note: Proj: Project.

Note:

1. Project Phase-2:

CIE marks shall be awarded by a committee comprising of HoD as Chairman, Guide/co-guide, if any and a Senior faculty of the department. The CIE marks awarded for project work phase -2, shall be based on the evaluation of Project Report subjected to plagiarism check, Project Presentation skill and Question and Answer session in the ratio 50:25:25.

SEE shall be at the end of IV semester. Project work evaluation and Viva-Voce examination (SEE), after satisfying the plagiarism check, shall be as per the University norms.

M.Tech 2018-Digital Electronics/ Electronics – FIRST SEMESTER SYLLABUS

ADVANCED ENGINEERING MATHEMATICS [As per Choice Based Credit System (CBCS) scheme] SEMESTER – I			
Subject	**18ELD11**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- To learn principles of advanced engineering mathematics through linear algebra and calculus of variations.
- To understand probability theory and random process that serve as an essential tool for applications of electronics and communication engineering sciences.

Modules	**RBT Level**
Module -1	
Linear Algebra-I Introduction to vector spaces and sub-spaces, definitions, illustrative example. Linearly independent and dependent vectors- Basis-definition and problems. Linear transformations-definitions. Matrix form of linear transformations-Illustrative examples (Text Book:1).	**L1, L2**
Module -2	
Linear Algebra-II Computation of eigen values and eigen vectors of real symmetric matrices-Given's method. Orthogonal vectors and orthogonal bases. Gram-Schmidt orthogonalization process (Text. Book:1).	**L1, L2**
Module -3	
Calculus of Variations : - Concept of functional-Eulers equation**.** Functional dependent on first and higher order derivatives, Functional on several dependent variables. Isoperimetric problems-variation problems with moving boundaries.	**L1, L2**
Module -4	

Probability Theory:-Review of basic probability theory. Definitions of random variables and probability distributions, probability mass and density functions, expectation, moments, central moments, characteristic functions, probability generating and moment generating functions-illustrations. Poisson, Gaussian and Erlang distributions-examples. (Text Book: 3)	**L1, L2**
Module -5	
Engineering Applications on Random processes:- Classification. Stationary, WSS and ergodic random process. Auto-correlation function-properties, Gaussian random process. (Text Book: 3)	**L2, L3, L4**

Course Outcomes: After studying this course, students will be able to:

CO-1: Understand vector spaces, basis, linear transformations and the process of obtaining
matrix of linear transformations arising in magnification and rotation of images.

CO-2: Apply the technique of singular value decomposition for data compression, least square approximation in solving inconsistent linear systems.

CO-3: Utilize the concepts of functional and their variations in the applications of communication systems, decision theory, synthesis and optimization of digital circuits.

CO-4: Learn the idea of random variables (discrete/continuous) and probability distributions in analyzing the probability models arising in control systems and system communications.

CO-5: Analyze random process through parameter-dependent variables in various random processes.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. David C.Lay, Steven R.Lay and J.J.McDonald: "LinearAlgebra and its Applications",
   5thEdition, Pearson Education Ltd., 2015
2. Elsgolts, L.:"Differential Equations and Calculus of Variations", MIR Publications, 3rdEdition, 1977.
3. T.Veerarajan: "Probability, Statistics and Random Process",3rd Edition,Tata Mc-Graw Hill Co.,2016.

Reference Books:

1. Gilbert Strang: Introduction to Linear Algebra, 5thEdition, Wellesley-Cambridge Press., 2016
2. Richard Bronson: "Schaum's Outlines of Theory and Problems of Matrix Operations", McGraw-Hill, 1988.
3. Scott L.Miller,DonaldG.Childers: "Probability and Random Process with application to Signal Processing", Elsevier Academic Press,2nd Edition,2013.

Web links:

1. http://nptel.ac.in/courses.php?disciplineId=111
2. http://www.class-central.com/subject/math(MOOCs)
3. http://ocw.mit.edu/courses/mathematics/
4. www.wolfram.com

ADVANCED DIGITAL SIGNAL PROCESSING **[As per Choice Based Credit System (CBCS) Scheme]** **SEMESTER – I**			
Course Code	**18ECS12**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50** **(10 Hours per Module)**	**Exam Hours**	**03**
Credits – 04			

Course objectives: This course will enable students to

- Understand Multirate digital signal processing principles and its applications.
- Estimate the various spectral components present in the received signal using different spectral estimation methods such as Parametric and Nonparametric.
- Design and implement an optimum adaptive filter using LMS and RLS algorithms.
- Understand the concepts and mathematical representations of Wavelet transforms.

Modules	**RBT Levels**
Module-1	
Multirate Digital Signal Processing: Introduction, decimation by a factor 'D', Interpolation by a factor 'I', sampling rate conversion by a factor 'I/D', Implementation of sampling rate conversion, Multistage implementation of sampling rate conversion, Applications of multirate signal processing, Digital filter banks, two channel quadrature mirror filter banks, M-channel QMF bank. (Text 1)	L1, L2, L3
Module-2	
Linear prediction and Optimum Linear Filters: Random signals, Correlation Functions and Power Spectra, Innovations Representation of a Stationary Random Process. Forward and Backward Linear Prediction. Solution of the Normal Equations. The Levinson-Durbin Algorithm. Properties of the Linear Prediction-Error Filters. (Text 1)	L1, L2, L3
Module-3	
Adaptive filters: Applications of Adaptive Filters-Adaptive Channel Equalization, Adaptive noise cancellation, Linear Predictive coding of Speech Signals, Adaptive direct form FIR filters-The LMS algorithm, Properties of LMS algorithm. Adaptive direct form filters- RLS algorithm. (Text 1)	L1, L2, L3
Module-4	
Power Spectrum Estimation: Non parametric Methods for Power Spectrum Estimation - Bartlett Method, Welch Method, Blackman and Tukey Methods. **Parametric Methods for Power Spectrum Estimation:**	L1, L2, L3

Relationship between the auto correlation and the model parameters, Yule and Walker methods for the AR Model Parameters, Burg Method for the AR Model parameters, Unconstrained least-squares method for the AR Model parameters, Sequential estimation methods for the AR Model parameters, ARMA Model for Power Spectrum Estimation. (Text 1)	
Module-5	
WAVELET TRANSFORMS: The Age of Wavelets, The origin of Wavelets, Wavelets and other reality transforms, History of wavelets, Wavelets of the future. **Continuous Wavelet and Short Time Fourier Transform:** Wavelet Transform, Mathematical preliminaries, Properties of wavelets. Discrete Wavelet Transform: Haar scaling functions, Haar wavelet function, Daubechies Wavelets. (Chapters 1, 3 & 4 of Text 2)	L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

- Design adaptive filters for a given application
- Design multirate DSP Systems
- Implement adaptive signal processing algorithm
- Design active networks
- Understand advanced signal processing techniques, including multi-rate processing and time-frequency analysis techniques

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. "Digital Signal Processing, Principles, Algorithms and Applications", JohnG. Proakis, Dimitris G.Manolakis, Fourth edition, Pearson-2007.

2. Insight into Wavelets- from Theory to Practice", K.P Soman, Ramachandran, Resmi- PHI Third Edition-2010.

ADVANCED EMBEDDED SYSTEM
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – I

Subject	18EVE13	CIE Marks	40
Number of Lecture Hours/Week	04	SEE Marks	60
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Describe the hardware software co-design and firmware design approaches
- Explain the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- Program ARM CORTEX M3 using the various instructions, for different applications.

Modules	Revised Bloom's Taxonomy (RBT) Level
Module -1	
Embedded System: Embedded vs General computing system, classification, application and purpose of ES. Core of an Embedded System, Memory, Sensors, Actuators, LED, Opto coupler, Communication Interface, Reset circuits, RTC, WDT, Characteristics and Quality Attributes of Embedded Systems (Text 1: Selected Topics from Ch -1, 2, 3).	**L1, L2, L3**
Module -2	
Hardware Software Co-Design, embedded firmware design approaches, computational models, embedded firmware development languages, Integration and testing of Embedded Hardware and firmware, Components in embedded system development environment (IDE), Files generated during compilation, simulators, emulators and debugging (Text 1: Selected Topics From Ch-7, 9, 12, 13).	**L1, L2, L3**
Module -3	
ARM-32 bit Microcontroller: Thumb-2 technology and applications of ARM, Architecture of ARM Cortex M3, Various Units in the architecture, General Purpose Registers, Special Registers, exceptions, interrupts, stack operation, reset sequence (Text 2: Ch 1, 2, 3)	**L1, L2, L3**
Module -4	

Instruction Sets: Assembly basics, Instruction list and description, useful instructions, Memory Systems, Memory maps, Cortex M3 implementation overview, pipeline and bus interface (Text 2: Ch-4, 5, 6).	**L1, L2, L3**
Module -5	
Exceptions, Nested Vector interrupt controller design, Systick Timer, Cortex-M3 Programming using assembly and C language, CMSIS (Text 2: Ch-7, 8, 10).	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Explain the hardware software co-design and firmware design approaches.
- Acquire the knowledge of the architectural features of ARM CORTEX M3, a 32 bit microcontroller including memory map, interrupts and exceptions.
- Apply the knowledge gained for Programming ARM CORTEX M3 for different applications.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. K. V. Shibu, "Introduction to embedded systems", TMH education Pvt. Ltd. 2009.

2. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edn, Newnes, (Elsevier), 2010.

Reference Book:

James K. Peckol, "Embedded systems- A contemporary design tool", John Wiley, 2008.

DIGITAL CIRCUITS AND LOGIC DESIGN
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – I

Course Code	**18ELD14**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

Credits – 04

Course objectives: This course will enable students to:

- Understand the concepts of sequential machines
- Design Sequential Machines/Circuits
- Analyze the faults in the design of circuits
- Apply fault detection experiments to sequential circuits

Modules	**RBT Levels**
Module-1	
Threshold Logic: Introductory Concepts, Synthesis of Threshold Networks, Capabilities, Minimization, and Transformation of Sequential Machines: The Finite- State Model, Further Definitions, Capabilities.	**L1, L2,L3**
Module-2	
Fault Detection by Path Sensitizing, Detection of Multiple Faults, Failure-Tolerant Design, Quadded Logic, Reliable Design and Fault Diagnosis Hazards: Fault Detection in Combinational Circuits.	**L1, L2, L3**
Module-3	
Fault-Location Experiments, Boolean Differences, Limitations of Finite – State Machines, State Equivalence and Machine Minimization, Simplification of Incompletely Specified Machines.	**L1, L2, L3**
Module-4	
Structure of Sequential Machines: Introductory Example, State Assignments Using Partitions, The Lattice of closed Partitions, Reductions of the Output Dependency, Input Independence and Autonomous Clocks, Covers and Generation of closed Partitions by state splitting, Information Flow in Sequential Machines, ELD ecompositions, Synthesis of Multiple Machines.	**L1, L2, L3**
Module-5	

State Identifications and Fault-Detection Experiments: Homing Experiments, Distinguishing Experiments, Machine Identification, Fault Detection Experiments, Design of Diagnosable Machines, Second Algorithm for the Design of Fault Detection Experiments, Fault-Detection.	**L1, L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Understand the concepts of sequential machines
- Design Sequential Machines/Circuits
- Analyze the faults in the design of circuits
- Apply fault detection experiments to sequential circuits

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Zvi Kohavi, "Switching and Finite Automata Theory", 2nd Edition, TMH, 2008, ISBN: 978_0_07_099387_7

Reference Books:

1. Charles Roth Jr., "Digital Circuits and logic Design", 7thedn, Cengage Learning, 2014.
2. Parag K Lala, "Fault Tolerant And Fault Testable Hardware Design", Prentice Hall Inc. 1985.
3. E. V. Krishnamurthy, "Introductory Theory of Computer", Macmillan Press Ltd, 1983
4. Mishra & Chandrasekaran, "Theory of computer science – Automata, Languages and Computation", 2nd Edition, PHI, 2004.

DIGITAL VLSI DESIGN [As per Choice Based Credit System (CBCS) scheme] SEMESTER –I			
Subject	**18EVE15**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- Explain VLSI Design Methodologies
- Learn Static and Dynamic operation principles, analysis and design of inverter circuit.
- Infer state of the art Semiconductors Memory circuits.
- Outline the comprehensive coverage of Methodologies and Design practice that are used to reduce the Power Dissipation of large scale digital circuits.
- Illustrate VLSI and ASIC design
- Illustrate VLSI and ASIC design.

Modules	**Revised Bloom's Taxonomy (RBT) Level**
Module -1	
MOS Transistor: The Metal Oxide Semiconductor (MOS) Structure, The MOS System under External Bias, Structure and Operation of MOS Transistor, MOSFET Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effects. **MOS Inverters-Static Characteristics**: Introduction, Resistive-Load Inverter, Inverters with n_Type MOSFET Load.	**L1, L2**
Module -2	
MOS Inverters-Static Characteristics: CMOS Inverter. **MOS Inverters**: Switching Characteristics and Interconnect Effects: Introduction, Delay-Time Definition, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters.	**L2, L3**
Module -3	
Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, Ferroelectric Random Access Memory (FRAM).	**L1, L2, L3**

Module -4	
Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques,High Performance Dynamic CMOS circuits. **BiCMOS Logic Circuits**: Introduction, Bipolar Junction Transistor (BJT): Structure and Operation, Dynamic Behavior of BJTs, Basic BiCMOS Circuits: Static Behavior, Switching Delay in BiCMOS Logic Circuits, BiCMOS Applications.	**L1,L2, L3**
Module -5	
Chip Input and Output (I/O) Circuits: Introduction, ESD Protection, Input Circuits, Output Circuits and L(di/dt) Noise, On-Chip Clock Generation and Distribution, Latch-Up and Its Prevention. **Design for Manufacturability:** Introduction, Process Variations, Basic Concepts and Definitions, Design of Experiments and Performance Modeling.	**L2, L3**

Course outcomes: After studying this course, students will be able to:

1. Analyse issues of On-chip interconnect Modelling and Interconnect delay calculation.
2. Analyse the Switching Characteristics in Digital Integrated Circuits.
3. Use the Dynamic Logic circuits in state-of-the-art VLSI chips.
4. Study critical issues such as ESD protection, Clock distribution, Clock buffering, and Latch phenomenon
5. Use Bipolar and Bi-CMOS circuits in very high speed design.

Question Paper Pattern

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Sung Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, Third Edition.

Reference Books:

1. Neil Weste and K. Eshragian, "Principles of CMOS VLSI Design: A System Perspective", Second Edition, Pearson Education (Asia) Pvt. Ltd. 2000.
2. Wayne, Wolf, "Modern VLSI Design: System on Silicon" Prentice Hall PTR/Pearson Education, Second Edition, 1998.
3. Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design" PHI 3rd Edition (original Edition – 1994).

EMBEDDED SYSTEMS LAB [As per Choice Based Credit System (CBCS) scheme] SEMESTER – I			
Laboratory Code	**18ELDL16**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**01Hr Tutorial (Instructions)+ 03 Hours Laboratory**	**Exam Marks**	**60**
		Exam Hours	**03**

CREDITS – 02

Course objectives: This laboratory course enables students to get practical experience on the

- Understand the design tool such as Cadence OrCAD/ OrCAD Lite /EDA tool
- Design of analog and digital circuits using the simulation tool
- Use of assembly level programming for different applications using ARM-CORTEX M3 Kit and Keil uVision-4 tool.
- Practice the different concepts and applications of C programming environment with ARM CORTEX M3.

Laboratory Experiments	**Revised Bloom's Taxonomy (RBT) Level**
Part A: EDA **Using Cadence OrCAD or OrCAD Lite or any EDA Tool, design and verify the following:** a) 3½ Digit Digital Voltmeter b) Monolithic function Generator c) Regulated Power supplies d) Batch counter using TTL ICs. e) DAC and ADC f) P, PI, PID and ON/OFF Controllers g) Programmable Timers h) Filters and Resonance Circuits	**L2,L3,L4**

PART-B: ARM-CORTEX M3 **[Programming to be done using Keil uVision 4 and download the program on to a M3 evaluation board such as NXP LPC1768 or ATMEL ATSAM3U]** a) Write an Assembly language program to calculate 10+9+8+.....+1 b) Write a Assembly language program to link Multiple object files and link them together. c) Write a Assembly language program to store data in RAM. d) Write a C program to Output the "Hello World" message using UART. e) Write a C program to Design a Stopwatch using interrupts. f) Write an Exception vector table in C g) Write an Assembly Language Program for locking a Mutex. h) Write a SVC handler in C. Use the wrapper code to extract the correct stack frame starting location. The C handler can then use this to extract the stacked PC location and the stacked register values.	L3

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Understand the computer aided design tools for the electronic circuit designs.
- Design an analog and digital systems using Cadence OrCAD, OrCAD Lite or any EDA tool.
- Develop assembly programs for different applications using ARM Cortex M3 and Keil uVision-4 tool.
- Develop C Programs for different applications using ARM-Cortex M3 and Keil uVision-4 tool.

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. For examination, two questions using different tool to be set.
3. Students are allowed to pick one experiment from the lot.
4. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
5. Change of experiment is allowed only once and Marks allotted to the procedure part to be made zero.

RESEARCH METHODOLOGY AND IPR

[As per Choice Based Credit System (CBCS) scheme]
SEMESTER –I

Course Code	18RMI17	CIE Marks	40
Number of Lecture Hours/Week	02	Exam Hours	03
Total Number of Lecture Hours	25	SEE Marks	60
Credits - 02			

Course objectives:

- To give an overview of the research methodology and explain the technique of defining a research problem
- To explain the functions of the literature review in research.
- To explain carrying out a literature search, its review, developing theoretical and conceptual frameworks and writing a review.
- To explain various research designs and their characteristics.
- To explain the details of sampling designs, and also different methods of data collections.
- To explain the art of interpretation and the art of writing research reports.
- To explain various forms of the intellectual property, its relevance and business impact in the changing global business environment.
- To discuss leading International Instruments concerning Intellectual Property Rights.■

Module-1	**Teaching Hours/ RBT Level**
Research Methodology: Introduction, Meaning of Research, Objectives of Research, Motivation in Research, Types of Research, Research Approaches, Significance of Research, Research Methods versus Methodology, Research and Scientific Method, Importance of Knowing How Research is Done, Research Process, Criteria of Good Research, and Problems Encountered by Researchers in India. ■	**05** **L1, L2**
Module-2	
Defining the Research Problem: Research Problem, Selecting the Problem, Necessity of Defining the Problem, Technique Involved in Defining a Problem, An Illustration. **Reviewing the literature:** Place of the literature review in research, Bringing clarity and focus to your research problem, Improving research methodology, Broadening knowledge base in research area, Enabling contextual findings, How to review the literature, searching the existing literature, reviewing the selected literature, Developing a theoretical framework, Developing a conceptual framework, Writing about the literature reviewed. ■	**05** **L1, L2**
Module-3	

Research Design: Meaning of Research Design, Need for Research Design, Features of a Good Design, Important Concepts Relating to Research Design, Different Research Designs, Basic Principles of Experimental Designs, Important Experimental Designs. **Design of Sample Surveys:** Introduction, Sample Design, Sampling and Non-sampling Errors, Sample Survey versus Census Survey, Types of Sampling Designs. ■	**05** **L1, L2**
Module-4	
Data Collection: Experimental and Surveys, Collection of Primary Data, Collection of Secondary Data, Selection of Appropriate Method for Data Collection, Case Study Method. **Interpretation and Report Writing:** Meaning of Interpretation, Technique of Interpretation, Precaution in Interpretation, Significance of Report Writing, Different Steps in Writing Report, Layout. **Interpretation and Report Writing (continued):** of the Research Report, Types of Reports, Oral Presentation, Mechanics of Writing a Research Report, Precautions for Writing Research Reports. ■	**05** **L1, L2, L3, L4**
Module-5	
Intellectual Property: The Concept, Intellectual Property System in India, Development of TRIPS Complied Regime in India, Patents Act, 1970, Trade Mark Act, 1999,The Designs Act, 2000, The Geographical Indications of Goods (Registration and Protection) Act1999, Copyright Act,1957,The Protection of Plant Varieties and Farmers' Rights Act, 2001,The Semi-Conductor Integrated Circuits Layout Design Act, 2000, Trade Secrets, Utility Models, IPR and Biodiversity, The Convention on Biological Diversity (CBD) 1992, Competing Rationales for Protection of IPRs, Leading International Instruments Concerning IPR, World Intellectual Property Organisation (WIPO),WIPO and WTO, Paris Convention for the Protection of Industrial Property, National Treatment, Right of Priority, Common Rules, Patents, Marks, Industrial Designs, Trade Names, Indications of Source, Unfair Competition, Patent Cooperation Treaty (PCT), Advantages of PCT Filing, Berne Convention for the Protection of Literary and Artistic Works, Basic Principles, Duration of Protection, Trade Related Aspects of Intellectual Property Rights(TRIPS) Agreement, Covered under TRIPS Agreement, Features of the Agreement, Protection of Intellectual Property under TRIPS, Copyright and Related Rights, Trademarks, Geographical indications, Industrial Designs, Patents, Patentable Subject Matter, Rights Conferred, Exceptions, Term of protection, Conditions on Patent Applicants, Process Patents, Other Use without Authorization of the Right Holder, Layout-Designs of Integrated Circuits, Protection of Undisclosed Information, Enforcement of Intellectual Property Rights, UNSECO.■	**05** **L1, L2, L3, L4**

Course outcomes:

At the end of the course the student will be able to:

- Discuss research methodology and the technique of defining a research problem
- Explain the functions of the literature review in research, carrying out a literature search, developing theoretical and conceptual frameworks and writing a review.
- Explain various research designs and their characteristics.
- Explain the art of interpretation and the art of writing research reports
- Discuss various forms of the intellectual property, its relevance and business impact in the changing global business environment and leading International Instruments concerning IPR.■

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

M.Tech 2018-Digital Electronics/ Electronics – SECOND SEMESTER SYLLABUS

ADVANCED COMPUTER ARCHITECTURE [As per Choice Based Credit System (CBCS) scheme] SEMESTER – II			
Subject Code	**18ELD21**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course objectives: This course will enable students to:

- Understand the basic concepts for parallel processing
- Analyze program partitioning and flow mechanisms
- Apply pipelining concept for the performance evaluation
- Learn the advanced processor architectures for suitable applications
- Know concepts of Parallel Programming

Modules	Revised Bloom's Taxonomy (RBT) Level
Module -1	
Parallel Computer Models: The State of Computing, Multiprocessors and multicomputers, Multivector and SIMD computers. **Program and Network Properties:** Conditions of parallelism, Program Partitioning & Scheduling, Program Flow Mechanisms.	**L1,L2, L3**
Module -2	
Principles of Scalable Performance: Performance Metrics and Measures, Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches. **Processors & Memory Hierarchy:** Advanced processor technology, Super Scalars & Vector Processors, Memory Hierarchy Technology, Virtual Memory Technology.	**L1,L2, L3,**
Module -3	
Bus, Cache and Shared Memory: Bus Systems, Cache Memory Organizations, Shared Memory Organizations, Sequential & Weak Consistency Model. **Pipelining & Superscalar Technologies:** Linear Pipeline Processors, Nonlinear Pipeline Processors, Instruction Pipeline Design, Arithmetic Pipeline Design, Superscalar Pipeline Design.	**L1, L2, L3**
Module -4	

Multivector & SIMD Computers: Vector Processing principles, Multivector Multiprocessors, Compound Vector Processing, SIMD Computer Organization. **Scalable, Multithreaded and Data Flow Computers:** Latency Hiding Techniques, Principles of Multithreading, Fine Grain Multi Computers, Scalable and Multithreaded Architectures, Data Flow and Hybrid Architectures.	**L1, L2, L3**
Module -5	
Parallel Models, Languages and Compilers: Parallel Programming Models, Parallel Languages & Compilers, Dependence Analysis and Data Arrays, Code Optimization and Scheduling, Loop Parallelization and Pipelining. **Parallel Program Development and Environments**: Parallel Programming Environments, Synchronization and Multi Processor Modes, Shared Variable Program Structures.	**L1, L2, L3**

Course outcomes: At the end of this course, the students will be able to:

- Understand the basic concepts for parallel processing
- Analyze program partitioning and flow mechanisms
- Apply pipelining concept for the performance evaluation
- Learn the advanced processor architectures for suitable applications
- Understand parallel Programming

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Kai Hwang & Narendra Jotwani, “Advanced Computer Architecture: Parallelism, Scalability, Programmability”, McGraw Hill Education, 3rd Edition, 2016, ISBN: 978-93-392-2092-1.

Reference Books:

1. M.J. Flynn, “Computer Architecture, Pipelined and Parallel Processor Design”, Narosa Publishing, 2002.
2. Michael J Quinn, “Parallel programming in C with MPI and OpenMP”, Tata McGraw Hill, 2013.
3. Ananth Grama “ An Introduction to Parallel Computing: Design and Analysis of Algorithms” 2nd Edn., Pearson, 2004.

Real Time Operating System [**As per Choice Based credit System (CBCS) Scheme** **SEMESTER – II**			
Subject Code	**18EVE22**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50(10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable the students to:

- Introduce the fundamental concepts of Real Time Operating Systems and the real time embedded system
- Apply concepts relating to operating systems such as Scheduling techniques, Thread Safe Reentrant Functions, Dynamic priority policies.
- Describe concepts related to Multi resource services like blocking, Deadlock, live lock & soft real-time services.
- Discuss Memory management concepts, Embedded system components, Debugging components and file system components.
- Study programs for multithreaded applications using suitable data structures.

Modules	**RBT Level**
Module 1	
Real-Time Systems and Resources: Brief history of Real Time Systems, A brief history of Embedded Systems. System Resources, Resource Analysis, Real-Time Service Utility, Scheduler concepts, Real-Time OS, State transition diagram and tables, Thread Safe Reentrant Functions. (Text 1: Selected sections from Chap. 1, 2)	L1,L2,L3
Module 2	
Processing with Real Time Scheduling: Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies with timing diagrams and problems and issues, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline –Monotonic Policy, Dynamic priority policies, Alternative to RM policy. (Text 1: Chap. 2,3,7)	L1,L2,L3
Module 3	
Memory and I/O: Worst case execution time, Intermediate I/O, Shared Memory, ECC Memory, Flash file systems. Multi-resource Services, Blocking, Deadlock and live lock, Critical sections to protect shared resources, Missed deadline, QoS, Reliability and Availability, Similarities and differences, Reliable software, Available software. (Text 1: Selected topics from Chap. 4,5,6,7,11)	L1,L2,L3
Module 4	
Firmware Components: The 3 firmware components, RTOS system software mechanisms, Software application components. Debugging	L1,L2,L3

Components, Exceptions, assert, Checking return codes, Single-step debugging, Test access ports, Trace Ports. (Text 1: Selected topics from Chap. 8,9)	
Module 5	
Process and Threads: Process and thread creations, Programs related to semaphores, message queue, shared buffer applications involving inter task/thread communication (Text 2: Chap. 11)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Develop programs for real time services, firmware and RTOS, using the fundamentals of Real Time Embedded System, real time service utilities, debugging methodologies and optimization techniques.
- Select the appropriate system resources (CPU, I/O, Memory, Cache, ECC Memory, Microcontroller/FPGA/ASIC to improve the system performance.
- Apply priority based static and dynamic real time scheduling techniques for the given specifications.
- Analyze deadlock conditions, shared memory problem, critical section problem, missed deadlines, availability, reliability and QoS.
- Develop programs for multithreaded applications using suitable techniques and data structure

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Sam Siewert, "Real-Time Embedded Systems and Components", Cengage Learning India Edition, 2007.

2. Dr. K.V.K.K Prasad, Embedded/Real Time Systems, Concepts, Design and Programming, Black Book, Dream Tech Press, New edition, 2010.

Reference Books:

1. James W S Liu, "Real Time System", Pearson education, 2008.
2. Dream Tech Software Team, "Programming for Embedded Systems", John Wiley, India Pvt. Ltd., 2008.

ERROR CONTROL CODING **[As per Choice Based Credit System (CBCS) Scheme]** **SEMESTER – 2**			
Subject Code	**18ECS23**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course objectives: This course will enable students to:

- Understand the concept of the Entropy, information rate and capacity for the Discrete memoryless channel.
- Apply modern algebra and probability theory for the coding.
- Compare Block codes such as Linear Block Codes, Cyclic codes etc and Convolutional codes.
- Detect and correct errors for different data communication and storage systems.
- Implement different Block code encoders and decoders.
- Analyze and implement convolutional encoders and decoders.
- Analyze and apply soft and hard Viterbi algorithm for decoding of convolutional codes.

Modules	**RBT Level**
Module 1	
Information theory: Introduction, Entropy, Source coding theorem, discrete memoryless channel, Mutual Information, Channel Capacity Channel coding theorem.(Chap. 5 of Text 1) **Introduction to algebra**: Groups, Fields, binary field arithmetic, Construction of Galois Fields GF (2^m) and its properties, (Only statements of theorems without proof) Computation using Galois filed GF (2^m) arithmetic, Vector spaces and Matrices. (Chap. 2 of Text 2)	L1,L2,L3
Module 2	
Linear block codes: Generator and parity check matrices, Encoding circuits, Syndrome and error detection, Minimum distance considerations, Error detecting and error correcting capabilities, Standard array and syndrome decoding, Single Parity Check Codes (SPC),Repetition codes, Self dual codes, Hamming codes, Reed-Muller codes. Product codes and Interleaved codes. (Chap. 3 of Text 2)	L1,L2,L3
Module 3	
Cyclic codes: Introduction, Generator and parity check polynomials, Encoding of cyclic codes, Syndrome computing and error detection, Decoding of cyclic codes, Error trapping Decoding, Cyclic hamming codes, Shortened cyclic codes.(Chap. 4 of Text2)	L1,L2,L3
Module 4	
BCH codes: Binary primitive BCH codes, Decoding procedures,	

Implementation of Galois field arithmetic. (Chap. 6 (6.1,6.2,6.7) of Text 2) Primitive BCH codes over GF (q), **Reed -Solomon codes.** (Chap. 7 (7.2,7.3) of Text 2) **Majority Logic decodable codes**: One -step majority logic decoding, Multiple-step majority logic. (Chap. 8 (8.1,8.4) of Text 2)	L1,L2,L3
Module 5	
Convolution codes: Encoding of convolutional codes: Systematic and Nonsystematic Convolutional Codes, Feedforward encoder inverse, A catastrophic encoder, Structural properties of convolutional codes: state diagram, state table, state transition table, tree diagram, trellis diagram. Viterbi algorithm, Sequential decoding: Log Likelihood Metric for Sequential Decoding. (11.1,11.2, 12.1,13.1 of Text 2)	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Analyse a discrete memoryless channel, given the source and transition probabilities.
- Apply the concept of modern linear algebra for the error control coding technique.
- Construct and Implement efficient LBC, Cyclic codes etc encoder and decoders.
- Apply decoding algorithms for efficient decoding of Block codes and Convolutional codes.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Simon Haykin, ”Digital Communication systems”, First edition, Wiley India Private. Ltd, 2014. ISBN 978-81-265-4231-4
2. Shu Lin and Daniel J. Costello. Jr, "Error control coding", Pearson, Prentice Hall, 2nd edition, 2004.

Reference Books:

1. Blahut. R. E, "Theory and practice of error control codes", Addison Wesley, 1984.
2. Salvatore Gravano, “Introduction to Error control coding”, Oxford university press, 2007.
3. Bernard Sklar, ”Digital Communications - Fundamentals and Applications”, 2nd Edition Pearson Education (Asia) Ptv. Ltd, 2001.

DIGITAL CIRCUITS SIMULATION LAB
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – II

Laboratory Code	**18ELDL26**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**01Hr Tutorial (Instructions)+ 03 Hours Laboratory**	**SEE Marks**	**60**
		Exam Hours	**03**

CREDITS – 02

Course objectives: This laboratory course enables students to

- Design and simulate digital electronic circuits using graphical programming tool LabVIEW.
- Create user friendly interfaces using LabVIEW and analyze the input and output data for various digital circuits.
- Understand the FPGA Design and testing for digital circuits
- Design of digital circuits using Verilog programming
- Verification and performance testing of digital circuits

Laboratory Experiments	**Revised Bloom's Taxonomy (RBT) Level**
PART-A: Graphical Programming using LabVIEW a) Design of 4 bit Adders (CLA, CSA, CMA, Parallel adders) b) Design of Binary Subtractors c) Design of Encoder (8X3), Decoder(3X8) d) Design of Multiplexer (8X1), and Demultiplexer (1X8) e) Design of code converters & Comparator f) Design of FF (SR, D, T, JK, and Master Slave with delays) g) Design of registers using latches and flip-flops h) Design of 8 bit Shift registers i) Design of Asynchronous & Synchronous Counters	L3

2. Develop Verilog Program for design and testing the following digital circuits (for 4/8 bits) using FPGA/CPLD. Use logic analyzer/Chipscope for the verification of results. **(Note:** Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels and logic analyzer)/Chipscope pro. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.) a. Carry skip and carry look ahead adder b. BCD adder and subtractor c. Array Multiplication (signed and unsigned) d. Booth multiplication (radix-4) e. Magnitude comparator f. LFSR g. Parity generator h. Universal Shift Register i. Sequence generation (11101 say) using Mealy/Moore FSM	**L2, L3, L4**

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Simulate the digital circuits using graphical programming tool LabVIEW.
- Build user friendly interfaces to interact with the digital circuits and to observe the outputs.
- Develop Verilog Programs for Digital Circuit design simulation and implement digital systems on FPGA/CPLD
- Testing and validation of digital systems using Logic analyzer/Chipscope

Conduct of Practical Examination:

1. All laboratory experiments are to be included for practical examination.
2. For examination, one question each to be set from PART-A and PART-B.
3. Students are allowed to pick one experiment from the lot.
4. Strictly follow the instructions as printed on the cover page of answer script for breakup of marks.
5. Change of experiment is allowed only once and Marks allotted to the procedure part will be made zero.

Professional Elective 1

Wireless Sensor Networks **[As per Choice Based Credit System (CBCS) scheme]** **SEMESTER – II**			
Course Code	**18ECS241**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
Credits – 04			

Course Outcomes:

At the end of this course, students will be able to

- Understand the hardware details of different types of sensors and select right type of sensor for various applications.
- Understand conversion of sensor information into digital data and packetize to a specific protocol for Transmission
- Understand radio standards and communication protocols to be used for wireless sensor.
- Understand the issues involved in synchronization and security.

Modules	RBT Levels
Module-1	
Motivation for a Network of Wireless Sensor Nodes Sensing and Sensors, Wireless Sensor Networks, Challenges and Constraints (Chapt 1 till 1.2.7) **Applications:**Structural Health Monitoring (till 2.1.4), Traffic Control (2.2), Health Care (2.3), Pipeline Monitoring (2.4), Precision Agriculture (2.5)	L1, L2, L3
Module-2	
Sensing Node Architecture: The Sensing Subsystem (3.1),The Processor (3.2) Subsystem (3.2) (in brief only), Communication Interfaces (3.3), Prototypes (3.4) **Medium Access Control :**Overview - Contention-Free Medium Access, Contention-Based Medium Access (6.1), Wireless MAC Protocols – CSMA, MACA and MACAW, MACA By Invitation, IEEE 802.11, IEEE 802.15.4 and ZigBee (6.2), Characteristics of MAC Protocols in Sensor Networks (6.3), Contention-Free MAC Protocols (6.4), Contention-Based MAC Protocols (6.5), Hybrid MAC Protocols (6.6)	L1, L2, L3
Module-3	
Network Layer: 7.1 Overview , 7.2 Routing Metrics, 7.3 Flooding and Gossiping, 7.4 Data-Centric Routing, 7.5 Proactive Routing, 7.6 On-Demand Routing, 7.8 Location-Based Routing , 7.9 QoS-Based Routing Protocols	L1, L2, L3
Module-4	

Power management: 8.1 Local Power Management Aspects, 8.2 Dynamic Power Management, 8.3 Conceptual Architecture. **Time Synchronization:** 9.1 Clocks and the Synchronization Problem, 9.2 Time Synchronization in Wireless Sensor Networks, 9.3 Basics of Time Synchronization,9.4 Time Synchronization Protocols till (9.4.5)	L1, L2, L3
Module-5	
Localization: 10.1 Overview, 10.2 Ranging Techniques, 10.3 Range-Based Localization, 10.4 Range-Free Localization, 10.5 Event-Driven Localization. **Network Security**: 11.1Fundamentals of Network Security, 11.2 Challenges of Security in Wireless Sensor Networks, 11.3 Security Attacks in Sensor	L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

CO1: Explain the concepts of sensors and conversion to digitally formatted signal for transmission.

CO2: Evaluate the capacity and degradation in performance of various wireless MAC protocols in a transmission environment.

CO3: Analyze schemes to transport sensor data to a server in a power efficient and time efficient manner.

CO4: Develop and evaluate the performance of a sensor network including localization of sensor faults.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as see marks is 60.

Text Book:

1. **WaltenegusDargie and Christian Poellabauer,** "Fundamentals of Wireless Sensor Networks Theory and Practice", John Wiley & Sons Ltd.ISBN 978-0-470-99765-9, 2010.

Reference Book:

1. **Ian F. Akyildiz** and **Mehmet Can Vuran** "Wireless Sensor Networks",John Wiley & Sons Ltd. ISBN 978-0-470-03601-3 (H/B), 2010.

NANOELECTRONICS
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – II

Subject Code	18EVE242	CIE	40
Number of Lecture Hours/Week	04	SEE Marks	60
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

CREDITS – 04

Course objectives: This course will enable students to:

- Enhance basic engineering science and technological knowledge of nanoelectronics .
- Explain basics of top-down and bottom-up fabrication process, devices and systems.
- Describe technologies involved in modern day electronic devices.
- Appreciate the complexities in scaling down the electronic devices in the future.

Modules	(RBT) Level
Module -1	
Introduction: Overview of nanoscience and engineering. Development milestones in microfabrication and electronic industry. Moores' law and continued miniaturization, Classification of Nanostructures, Electronic properties of atoms and solids: Isolated atom, Bonding between atoms, Giant molecular solids, Free electron models and energy bands, crystalline solids, Periodicity of crystal lattices, Electronic conduction, effects of nanometer length scale, Fabrication methods: Top down processes, Bottom up processes methods for templating the growth of nanomaterials, ordering of nanosystems (Text 1).	**L1, L2**
Module -2	
Characterization: Classification, Microscopic techniques, Field ion microscopy, scanning probe techniques, diffraction techniques: bulk and surface diffraction techniques,spectroscopy techniques: photon, radiofrequency, electron, surface analysis and dept profiling: electron, mass, Ion beam, Reflectrometry, Techniques for property measurement: mechanical, electron, magnetic, thermal properties(Text1)	**L1,L2,L3**
Module -3	

Inorganic semiconductor nanostructures: overview of semiconductor physics. Quantum confinement in semiconductor nanostructures: quantum wells, quantum wires, quantum dots, super-lattices, band offsets, electronic density of states (Text1). **Carbon Nanostructures:**Carbon molecules, Carbon Clusters, Carbon Nanotubes, application of Carbon Nanotubes (Text 2).	**L1, L2, L3**
Module -4	
Fabrication techniques: requirements of ideal semiconductor, epitaxial growth of quantum wells, lithography and etching, cleaved-edge over growth, growth of vicinal substrates, strain induced dots and wires, electrostatically induced dots and wires, Quantum well width fluctuations, thermally annealed quantum wells, semiconductor nanocrystals, collidal quantum dots, self-assembly techniques. **Physical processes:** modulation doping, quantum hall effect, resonant tunneling, charging effects, ballistic carrier transport, Inter band absorption, intra band absorption, Light emission processes, phonon bottleneck, quantum confined stark effect, nonlinear effects, coherence and dephasing, characterization of semiconductor nanostructures: optical electrical and structural (Text1).	**L1, L2, L3**
Module -5	
Methods of measuring properties: atomic, crystollography, microscopy, spectroscopy (Text 2). **Applications**: Injection lasers, quantum cascade lasers, single-photon sources, biological tagging, optical memories, coulomb blockade devices, photonic structures, QWIP's, NEMS, MEMS (Text1).	**L1, L2, L3**

Course outcomes: After studying this course, students will be able to:

1. Know the principles behind Nanoscience engineering and Nanoelectronics.
2. Apply the knowledge to prepare and characterize nanomaterials.
3. Know the effect of particles size on mechanical, thermal, optical and electrical properties of nanomaterials.
4. Design the process flow required to fabricate state of the art transistor technology.
5. Analyze the requirements for new materials and device structure in the future tech nologies.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Ed Robert Kelsall, Ian Hamley, Mark Geoghegan, "Nanoscale Science and Technology", John Wiley, 2007.
2. Charles P Poole, Jr, Frank J Owens, "Introduction to Nanotechnology", John Wiley, Copyright 2006, Reprint 2011.

Reference Book:

- Ed William A Goddard III, Donald W Brenner, Sergey E. Lyshevski, Gerald J Iafrate, "Hand Book of Nanoscience Engineering and Technology", CRC press, 2003.

CRYPTOGRAPHY AND NETWORK SECURITY
[As per Choice Based credit System (CBCS) Scheme]
SEMESTER – II

Subject Code	**18ECS243**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours Per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Understand the basics of symmetric key and public key cryptography.
- Understand some basic mathematical concepts and pseudorandom number generators required for cryptography.
- Authenticate and protect the encrypted data.
- Enrich knowledge about Email, IP and Web security.

Modules	**RBT Level**
Module 1	
Foundations: Terminology, Steganography, substitution ciphers and transpositions ciphers, Simple XOR, One-Time Pads, Computer Algorithms (Text 2: Chapter 1: Section 1.1 to 1.6) **SYMMETRIC CIPHERS:** Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher. (Text 1: Chapter 2: Section2.1, 2.2, Chapter 4)	L1,L2,L3
Module 2	
Introduction to modular arithmetic, Prime Numbers, Fermat's and Euler's theorem, primality testing, Chinese Remainder theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 3, 4, 5) Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography (Text 1: Chapter 8, Chapter 9: Section 9.1, 9.3, 9.4)	L1,L2,L3
Module 3	
Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M, PKZIP (Text 2: Chapter 16)	L1,L2, L3
Module 4	
One-Way Hash Functions: Background, Snefru, N-Hash, MD4, MD5, Secure Hash Algorithm [SHA],One way hash functions using symmetric block algorithms, Using public key algorithms, Choosing a one-way hash functions, Message Authentication Codes. Digital Signature Algorithm, Discrete Logarithm Signature Scheme (Text 2: Chapter 18: Section 18.1 to 18.5, 18.7, 18.11 to 18.14 and Chapter 20: Section 20.1, 20.4)	L1,L2,L3

Module 5	
E-mail Security: Pretty Good Privacy-S/MIME (Text 1: Chapter 17: Section 17.1, 17.2). **IP Security:** IP Security Overview, IP Security Policy, Encapsulation Security Payload (ESP), Combining security Associations. (Text 1: Chapter 18: Section 18.1 to 18.4). **Web Security:** Web Security Considerations, SSL (Text 1: Chapter 15: Section 15.1, 15.2).	L1,L2, L3

Course Outcomes: After studying this course, students will be able to:

- Use basic cryptographic algorithms to encrypt the data.
- Generate some pseudorandom numbers required for cryptographic applications.
- Provide authentication and protection for encrypted data.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X

Reference Books:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

Professional Elective 2

AUTOMOTIVE ELECTRONICS **[As per Choice Based credit System (CBCS) Scheme** **SEMESTER – II**			
Subject Code	**18EIE251**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Understand the complete dynamics of automotive electronics
- Design and implement the electronics that attributes the smartness to the automobiles by way of unprecedented safety, add-on features, and comforts.

Modules	**RBT Level**
Module 1	
Automotive Fundamentals, the Systems Approach to Control and Instrumentation: Use Of Electronics In The Automobile, Antilock Brake Systems, (ABS), Electronic steering control, Power steering, Traction control, Electronically controlled suspension. (Chap.1 and 2 of Text)	L1,L2
Module 2	
Automotive instrumentation Control: Sampling, Measurement and signal conversion of various parameters. (Chap. 4 of Text)	L1,L2, L3
Module 3	
The basics of Electronic Engine control: Integrated body: Climate controls, Motivation for Electronic Engine Control, Concept of An Electronic Engine Control System, Definition of General Terms, Definition of Engine Performance Terms, Electronic fuel control system, Engine control sequence, Electronic Ignition, Sensors and Actuators, Applications of sensors and actuators, air flow rate sensor, Indirect measurement of mass air flow, Engine crankshaft angular position sensor, Automotive engine control actuators, Digital engine control, Engine speed sensor, Timing sensor for ignition and fuel delivery, Electronic ignition control systems, Safety systems, Interior safety, Lighting, Entertainment systems. (Chap. 5 and 6 of Text)	L1,L2,L3
Module 4	

Vehicle Motion Control and Automotive diagnostics: Cruise control system, Digital cruise control, Timing light, Engine analyzer, On-board and off-board diagnostics, Expert systems. Stepper motor-based actuator, Cruise control electronics, Vacuum - antilock braking system, Electronic suspension ystem Electronic steering control, Computer-based instrumentation system, Sampling and Input\output signal conversion, Fuel quantity measurement, Coolant temperature measurement, Oil pressure measurement, Vehicle speed measurement, Display devices, Trip-Information-Computer, Occupant protection systems. (Chap. 8 and 10 of Text)	L1,L2, L3
Module 5	
Future automotive electronic systems: Alternative Fuel Engines, Collision Wide Range Air/Fuel Sensor, Alternative Engine, Low Tire Pressure Warning System, Collision avoidance Radar Warning Systems, Low Tire Pressure Warning System, Radio Navigation, Advance Driver information System. Alternative-Fuel Engines , Transmission Control , Collision Avoidance Radar Warning System, Low Tire Pressure Warning System, Speech Synthesis Multiplexing in Automobiles, Control Signal Multiplexing, Navigation Sensors, Radio Navigation, Sign post Navigation , Dead Reckoning Navigation Future Technology, Voice Recognition Cell Phone Dialing Advanced Driver information System, Automatic Driving Control. (Chap. 11 of Text)	L1, L2, L3
Course Outcomes: After studying this course, students will be able to: • Implement various control requirements in the automotive system. • Comprehend dashboard electronics and engine system electronics. • Identify various physical parameters that are to be sensed and monitored for maintaining the stability of the vehicle under dynamic conditions. • Understand and implement the controls and actuator system pertaining to the comfort and safety of commuters. • Design sensor network for mechanical fault diagnostics in an automotive vehicle.	
Question paper pattern: • Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks. • Each full question can have a maximum of 4 sub questions. • There will be 2 full questions from each module covering all the topics of the module. • Students will have to answer 5 full questions, selecting one full question from each module. • The total marks will be proportionally reduced to 60 marks as SEE marks is 60.	

Text Book:

William B. Ribbens , "Understanding Automotive Electronics", SAMS/Elsevier publishing, 6th Edition, 1997.

Reference Book:

Robert Bosch Gmbh, "Automotive Electrics and Automotive Electronics-Systems and Components, Networking and Hybrid Drive", Springer Vieweg, 5th Edition, 2007.

SoC DESIGN [As per Choice Based credit System (CBCS) Scheme SEMESTER – II			
Subject Code	**18EVE252**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Describe the ARM processor architecture and user-level assembly language programming
- Appreciate what a high-level language (in this case, C) really needs and how those needs are met by the ARM instruction set.
- raises the issues involved in debugging systems which use embedded
- processor cores and in the production testing of board-level systems.
- Learn the concept of memory hierarchy, discussing the principles
- of memory management and caches.

Modules	RBT Level
Module 1	
ARM Organization and Implementation:3-stage pipeline ARM organization, 5-stage pipeline ARM organization, ARM instruction execution, ARM implementation, The ARM coprocessor interface. **The ARM Instruction Set :**Introduction, Exceptions, Conditional execution, Branch and Branch with Link (B, BL),Branch, Branch with Link and eXchange (BX, BLX),Software Interrupt (SWI),Data processing instructions, Multiply instructions, Count leading zeros (CLZ - architecture v5T only), Single word and unsigned byte data transfer instruction, Half-word and signed byte data transfer instructions ,Multiple register transfer instructions, Swap memory and register instructions (SWP), Status register to general register transfer instructions , General register to status register transfer instructions, Coprocessor instructions, Coprocessor data operations, Coprocessor data transfers, Coprocessor register transfers, Breakpoint instruction (BRK - architecture v5T only), Unused instruction space, Memory faults, ARM architecture variants.	L1,L2
Module 2	
Architectural Support for High-Level Languages: Abstraction in software design, Data types, Floating-point data types, The ARM floating-point architecture, Expressions, Conditional statements, Loops, Functions and procedures, Use of memory, Run-time environment. **Architectural Support for System Development:** The ARM	L1,L2

memory interface, The Advanced Microcontroller Bus Architecture (AMBA), The ARM reference peripheral specification, Hardware system prototyping tools, The ARMulator, The JTAG boundary scan test architecture, The ARM debug architecture, Embedded Trace, Signal processing support.	
Module 3	
ARM Processor Cores: ARM7TDMI, ARM8,ARM9TDMI, ARM10TDMI ,Discussion ,Example and exercises. **Memory Hierarchy:** Memory size and speed, On-chip memory, Caches, Cache design - an example, Memory management, Examples and exercises.	L1,L2
Module 4	
Architectural Support for Operating Systems: An introduction to operating systems, The ARM system control coprocessor, CP15 protection unit registers, ARM protection unit,CP15 MMU registers, ARM MMU architecture, Synchronization, Context switching, Input/ Output, Example and exercises. **ARM CPU Cores:** The ARM710T, ARM720T and ARM740T, The ARM810,The Strong ARM SA-110,The ARM920T and ARM940T,The ARM946E-S and ARM966E-S,The ARM1020E,Discussion,Example and exercises.	L1,L2
Module 5	
Embedded ARM Applications: The VLSI Ruby II Advanced Communication Processor, The VLSI ISDN Subscriber Processor, The One C™VWS22100 GSM chip, The Ericsson-VLSI Bluetooth Baseband Controller, The ARM7500 and ARM7500FE, The ARM7100 364,The SA-1100 368,Examples and exercises. **The AMULET Asynchronous ARM Processors:** Self-timed design 375,AMULET1 377,AMULET2 381,AMULET2e 384,AMULET3 387,The DRACO telecommunications controller 390, A self-timed future? 396, Example and exercises.	L1,L2,L3
Course Outcomes: After studying this course, students will be able to: 1. Apply the 3- and 5-stage pipeline ARM processor cores and analyse the implementation issues. 2. Use the concepts and methodologies employed in designing a System-on-chip (SoC) based around a microprocessor core and in designing the microprocessor core itself. 3. Understand how SoCs and microprocessors are designed and used, and why a modern processor is designed the way that it is. 4. Use integrated ARM CPU cores (including StrongARM) that incorporate full support for memory management. 5. Analyze the requirements of a modern operating system and use the ARM architecture to address the same.	
Question paper pattern: • Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks. • Each full question can have a maximum of 4 sub questions. • There will be 2 full questions from each module covering all the topics of the module.	

- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

- Steve Furber, “ARM System-On-Chip Architecture”, Addison Wesley, 2nd edition.

References Books:

1. Joseph Yiu, “The Definitive Guide to the ARM Cortex-M3”, 2nd edn, Newnes, (Elsevier), 2010.
2. Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System on Chip Interconnect”, Morgan Kaufmann, Publishers © 2008.
3. Michael Keating, Pierre Bricaud, “Reuse Methodology Manual for System on Chip designs”, Kluwer Accademic Publishers, 2nd edition, 2008.

MICRO ELECTRO MECHANICAL SYSTEMS
[As per Choice Based credit System (CBCS) Scheme
SEMESTER – II

Subject Code	**18ELD253**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Know an overview of microsystems, their fabrication and application areas.
- Teach working principles of several MEMS devices.
- Develop mathematical and analytical models of MEMS devices
- Know methods to fabricate MEMS devices
- Expose the students to various application areas where MEMS devices can be used.

Modules	**RBT Level**
Module 1	
Overview of MEMS and Microsystems: MEMS and Microsystem, Typical MEMS and Microsystems Products, Evolution of Microfabrication, Microsystems and Microelectronics, Multidisciplinary Nature of Microsystems, Miniaturization. Applications and Markets.	L1, L2
Module 2	
Working Principles of Microsystems: Introduction, Microsensors, Microactuation, MEMS with Microactuators, Microaccelerometers, Microfluidics. **Engineering Science for Microsystems Design and Fabrication:** Introduction, Atomic Structure of Matters, Ions and Ionization, Molecular Theory of Matter and Inter-molecular Forces, Doping of Semiconductors, The Diffusion Process, Plasma Physics, Electrochemistry.	L1, L2
Module 3	
Engineering Mechanics for Microsystems Design: Introduction, Static Bending of Thin Plates, Mechanical Vibration, Thermomechanics, Fracture Mechanics, Thin Film Mechanics, Overview on Finite Element Stress Analysis.	L1,L2,L3
Module 4	
Scaling Laws in Miniaturization: Introduction, Scaling in Geometry, Scaling in Rigid-Body	L1,L2,L3

Dynamics, Scaling in Electrostatic Forces, Scaling of Electromagnetic Forces, Scaling in Electricity, Scaling in Fluid Mechanics, Scaling in Heat Transfer.	
Module 5	
Overview of Micro-manufacturing: Introduction, Bulk Micro-manufacturing, Surface Micromachining, The LIGA Process, Summary on Micro-manufacturing. **Microsystem Design:** Introduction, Design Considerations, Process Design, Mechanical Design, Using Finite Element Method.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Understand the technologies related to Micro Electro Mechanical Systems.
- Describe the design and fabrication processes involved with MEMS devices.
- Analyse the MEMS devices and develop suitable mathematical models
- Understand the various application areas for MEMS devices

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Tai-Ran Hsu, MEMS and Micro systems: Design, Manufacture and Nanoscale Engineering, 2nd Ed, John Wiley & Sons, 2008. ISBN: 978-0-470-08301-7

Reference Books:

1. Hans H. Gatzen, Volker Saile, JurgLeuthold, Micro and Nano Fabrication: Tools and Processes, Springer, 2015.
2. Dilip Kumar Bhattacharya, Brajesh Kumar Kaushik, Micro electromechanical Systems (MEMS), Cenage Learning.

M.Tech 2018-Digital Electronics/ Electronics - THIRD SEMESTER SYLLABUS

SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS **[As per Choice Based Credit System (CBCS) scheme]** **SEMESTER – III**			
Course Code	**18ELD31**	**CIA Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
Credits – 04			

Course objectives: This course will enable students to

- Understand the need for optimization and dimensions of optimization for digital circuits.
- Understand basic optimization techniques used in circuits design
- Understand advanced tools and techniques in digital systems design including Hardware Modeling and Compilation Techniques.
- Explain details of Logic-Level synthesis and optimization techniques for combinational and sequential circuits.
- Explain the concept of scheduling and resource binding for optimization.

Modules	**RBT Levels**
Module-1	
Introduction to Synthesis and optimization: Design of Microelectronics circuits, Computer aided Synthesis and Optimization. **Hardware Modeling**: HDLs for Synthesis, Abstract models, Compilation and Behavioral Optimization. (Text1: Topics from Chap.1,3)	L1, L2, L3
Module-2	
Graph theory for CAD for VLSI: Graphs, Combinatorial Optimization, Graph Optimization problems and Algorithms, Boolean Algebra and Applications. **Architectural Synthesis and Optimization:** Fundamental Architectural Synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization, Datapath Synthesis, Control Path Synthesis.(Text1: Topics From Chap. 2,4)	L1, L2, L3
Module-3	
Two level Combinational Logic Optimization: Introduction, Logic Optimizations, Operations on Two level Logic Covers, Algorithms for Logic Minimization, Symbolic Minimization and Encoding Problems. **Multiple Level Combinational Logic Optimization**:	L1, L2, L3

Introduction, Models and Transformations for Combinational Networks, The Algebraic Model, The Boolean Model. (Text1: Chap. 7, 8)	
Module-4	
Sequential Logic Optimization: Introduction, Sequential Logic Optimization using State based Models, Sequential Logic Optimization using Network Models, Implicit FSM Traversal Methods, Testability concerns for Synchronous Circuits. (Text 1: Chap. 9)	L1, L2, L3
Module-5	
Scheduling Algorithms: Introduction, A Model for Scheduling problems, Scheduling with Resource Constraints, Scheduling without Resource Constraints, Scheduling Algorithms for Extended Sequencing Models, Scheduling Pipelined Circuits. **Resource Sharing and Binding:** Sharing and Binding for Resource dominated circuits, Sharing and Binding for General Circuits, Concurrent Binding and Scheduling. (Text1: Chap. 5,6)	L1, L2, L3

Course Outcomes: After studying this course, students will be able to:

- Understand the process of synthesis and optimization in a top down approach for digital circuits models using HDLs.
- Understand the terminologies of graph theory and its algorithms to optimize a Boolean equation.
- Apply different two level and multilevel optimization algorithms for combinational circuits
- Apply the different sequential circuit optimization methods using state models and network models.
- Apply different scheduling algorithms with resource binding and without resource binding for pipelined sequential circuits and extended sequencing models.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", Tata McGraw-Hill, 2003.ISBN: 9780070582781

Reference Books:

Edwars M.D., Automatic Logic synthesis Techniques for Digital Systems, Macmillan New Electronic Series, 1992.

Professional Elective 3

Advances in Image Processing **[As per Choice Based credit System (CBCS) Scheme** **SEMESTER – III**			
Subject Code	**18ECS321**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours Per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

1. Acquire fundamental knowledge in understanding the representation of the digital image and its properties
2. Equip with some pre-processing techniques required to enhance the image for further analysis purpose.
3. Select the region of interest in the image using segmentation techniques.
4. Represent the image based on its shape and edge information.
5. Describe the objects present in the image based on its properties and structure.

Modules	**RBT Level**
Module 1	
The image, its representations and properties: Image representations a few concepts, Image digitization, Digital image properties, Color images.	L1
Module 2	
Image Pre-processing: Pixel brightness transformations, geometric transformations, local pre-processing.	L1, L2
Module 3	
Segmentation: Thresholding; Edge-based segmentation – Edge image thresholding, Edge relaxation, Border tracing, Hough transforms; Region – based segmentation – Region merging, Region splitting, Splitting and merging, Watershed segmentation, Region growing post-processing.	L1, L2, L3
Module 4	
Shape representation and description: Region identification; Contour-based shape representation and description – Chain codes, Simple geometric border representation, Fourier transforms of boundaries, Boundary description using segment sequences, B-spline representation; Region-based shape representation and description – Simple scalar region descriptors, Moments, Convex hull.	L1, L2, L3
Module 5	
Mathematical Morphology: Basic morphological concepts, Four morphological principles, Binary dilation and erosion, Skeletons	L1, L2, L3

and object marking, Morphological segmentations and watersheds.	

Course Outcomes: After studying this course, students will be able to:

1.Understand the representation of the digital image and its properties
2.Apply pre-processing techniques required to enhance the image for its further analysis.
3.Use segmentation techniques to select the region of interest in the image for analysis
4.Represent the image based on its shape and edge information.
5.Describe the objects present in the image based on its properties and structure.
6.Use morphological operations to simplify images, and quantify and preserve the main shape characteristics of the objects.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Milan Sonka, Vaclav Hlavac, Roger Boyle, “Image Processing, Analysis, and Machine Vision”, Cengage Learning, 2013, ISBN: 978-81-315-1883-0

Reference Books:

1. Geoff Doughertry, Digital Image Processing for Medical Applications, Cambridge university Press, 2010
2. S.Jayaraman, S Esakkirajan, T.Veerakumar, Digital Image Processing, Tata McGraw Hill, 2011.

CMOS RF Circuit Design

[As per Choice Based credit System (CBCS) Scheme

SEMESTER – III

Subject Code	**18EVE322**	**IA Marks**	**40**
Number of Lecture Hours/Week	**04**	**Exam marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 04

Course Objectives: This course will enable students to:

- Learn basic concepts in RF and microwave design emphasizing the effects of nonlinearity and noise.
- Appreciate communication system, multiple access and wireless standards necessary for RF circuit design.
- Deal with transceiver architecture, various receiver and transmitter designs, their merits and demerits
- Understand the design of RF building blocks such as Low Noise Amplifiers, Mixers, Oscillators and PLLs

Modules	**RBT Level**
Module 1	
Introduction to RF Design, Wireless Technology and Basic Concepts: A wireless world, RF design is challenging, The big picture. General considerations, Effects of Nonlinearity, Noise, Sensitivity and dynamic range, Passive impedance transformation. Scattering parameters, Analysis of nonlinear dynamic systems, conversion of gains and distortion	L1,L2,L3
Module 2	
Communication Concepts: General concepts, analog modulation, digital modulation, spectral re-growth, coherent and non-coherent detection, Mobile RF communications, Multiple access techniques, Wireless standards, Appendix 1: Differential phase shift keying.	L1,L2,L3
Module 3	
Transceiver Architecture: General considerations, Receiver architecture, Transmitter architectures, Direct conversion and two-step transmitters, RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.	L1,L2,L3
Module 4	
Low Noise Amplifiers and Mixers: General considerations, Problem of input matching, LNA topologies: common-source stage with inductive load, common-source stage with resistive feedback. Mixers-General considerations, passive down conversion mixers, Various mixers-working and implementation	L1,L2,L3

Module 5	
VCO and PLLs- Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

1. Analyse the effect of nonlinearity and noise in RF and microwave design.
2. Exemplify the approaches taken in actual RF products.
3. Minimize the number of off-chip components required to design mixers, Low-Noise Amplifiers, VCO and PLLs.
4. Explain various receivers and transmitter topologies with their merits and drawbacks.
5. Demonstrate how the system requirements define the parameters of the circuits and the impact on the performance

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

B. Razavi, "**RF Microelectronics**", PHI, second edition.

Reference Books:

1. R. Jacob Baker, H.W. Li, D.E. Boyce "**CMOS Circuit Design, layout and Simulation**", PHI 1998.

2. Thomas H. Lee "**Design of CMOS RF Integrated Circuits**" Cambridge University press 1998.

3. Y.P. Tsividis, "**Mixed Analog and Digital Devices and Technology**", TMH 1996

Communication System Design using DSP Algorithms

[As per Choice Based Credit System (CBCS) scheme]

SEMESTER – III

Course Code	18ESP323	CIE Marks	40
Number of Lecture Hours/Week	04	SEE Marks	60
Total Number of Lecture Hours	50 (10 Hours per Module)	Exam Hours	03

Credits – 04

Course Objectives: This course will enable students to:

- Understand communication systems, including algorithms that are particularly suited to DSP implementation.
- Understand Software and hardware tools, as well as FIR and IIR digital filters and the FFT.
- Discuss modulators and demodulators for classical analog modulation methods such as amplitude modulation (AM), double-sideband suppressed-carrier amplitude modulation (DSBSC-AM), single sideband modulation (SSB), and frequency modulation (FM).
- Explore digital communication methods leading to the implementation of a telephone-line modem.

Modules	RBT Level
Module 1	
Introduction to the course: Digital filters, Discrete time convolution and frequency responses, FIR filters - Using circular buffers to implement FIR filters in C and using DSP hardware, Interfacing C and assembly functions, Linear assembly code and the assembly optimizer. IIR filters - realization and implementation, FFT and power spectrum estimation: DTFT window function, DFT and IDFT, FFT, Using FFT to implement power spectrum.	**L1,L2**
Module 2	
Analog modulation scheme: Amplitude Modulation - Theory, generation and demodulation of AM, Spectrum of AM signal. Envelope detection and square law detection. Hilbert transform and complex envelope, DSP implementation of amplitude modulation and demodulation. **DSBSC:** Theory generation of DSBSC, Demodulation, and demodulation using coherent detection and Costas loop. Implementation of DSBSC using DSP hardware. **SSB:** Theory, SSB modulators, Coherent demodulator, Frequency translation, Implementation using DSP hardware. (Text 1, 2)	**L1,L2**
Module 3	
Frequency modulation: Theory, Single tone FM, Narrow band FM, FM bandwidth, FM demodulation, Discrimination and PLL methods, Implementation using DSP hardware. **Digital Modulation scheme:** PRBS, and data scramblers: Generation of PRBS, Self -synchronizing data scramblers, Implementation of PRBS and	**L1,L2**

data scramblers. RS-232C protocol and BER tester: The protocol, error rate for binary signaling on the Gaussian noise channels, Three bit error rate tester and implementation.	
Module 4	
PAM and QAM: PAM theory, baseband pulse shaping and ISI, Implementation of transmit filter and interpolation filter bank. Simulation and theoretical exercises for PAM, Hardware exercises for PAM. **QAM fundamentals:** Basic QAM transmitter, 2 constellation examples, QAM structures using passband shaping filters, Ideal QAM demodulation, QAM experiment. QAM receivers-Clock recovery and other frontend sub-systems. Equalizers and carrier recovery systems.	**L2,L3**
Module 5	
Experiment for QAM receiver frontend. Adaptive equalizer, Phase splitting, Fractionally spaced equalizer. Decision directed carrier tracking, Blind equalization, Complex cross coupled equalizer and carrier tracking experiment. Echo cancellation for full duplex modems: Multicarrier modulation, ADSL architecture, Components of simplified ADSL transmitter, A simplified ADSL receiver, Implementing simple ADSL Transmitter and Receiver.	**L2,L3**

Course outcomes: After studying this course, students will be able to:

- Implement DSP algorithms on TI DSP processors
- Implement FIR, IIR digital filtering and FFT methods
- Implement modulators and demodulators for AM,DSBSC-AM,SSB and FM
- Design digital communication methods leading to the implementation of a line communication system.

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

1. Tretter, Steven A., “Communication System Design Using DSP Algorithms With Laboratory Experiments for the TMS320C6713™ DSK”, Springer USA, 2008.

Reference Books:

1. Robert. O. Cristi, "Modern Digital signal processing", Cengage Publishers, India, 2003.
2. S. K. Mitra, "Digital signal processing: A computer based approach", 3rd edition, TMH, India, 2007.
3. E.C. Ifeachor, and B. W. Jarvis, "Digital signal processing: A Practitioner's approach", Second Edition, Pearson Education, India, 2002,
4. Proakis, and Manolakis, "Digital signal processing", 3rd edition, Prentice Hall, 1996

Professional Elective 4

VLSI Design for Signal Processing [As per Choice Based credit System (CBCS) Scheme SEMESTER – III			
Subject Code	**18EVE331**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
CREDITS – 04			

Course Objectives: This course will enable students to:

- Learn several high-level architectural transformations that can be used to design families of architectures for a given algorithm.
- Deal with high-level algorithm transformations such as strength reduction, look-ahead and relaxed look-ahead.

Modules	**RBT Level**
Module 1	
Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms. **Iteration Bounds:** Data flow graph Representations, loop bound and Iteration bound. Algorithms for Computing Iteration Bound, Iteration Bound of multi rate data flow graphs.	L1, L2
Module 2	
Pipelining and Parallel Processing: pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power. **Retiming:** Definition and Properties, Solving Systems of Inequalities, Retiming Techniques.	L1,L2,L3
Module 3	
Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding. **Folding:** Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.	L1,L2,L3
Module 4	
Systolic Architecture Design: systolic array design Methodology, FIR systolic array, Selection of Scheduling Vector, Matrix-Matrix Multiplication and 2D systolic Array Design, Systolic Design for space representation containing Delays. **Fast convolution**: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.	L1,L2,L3
Module 5	

Pipelined and Parallel Recursive and Adaptive Filter: Pipeline Interleaving in Digital Filter, first order IIR digital Filter, Higher order IIR digital Filter, parallel processing for IIR filter, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing, pipelined adaptive digital filter.	L1,L2,L3

Course Outcomes: After studying this course, students will be able to:

- Illustrate the use of various DSP algorithms and addresses their representation using block diagrams, signal flow graphs and data-flow graphs
- Use pipelining and parallel processing in design of high-speed /low-power applications
- Apply unfolding in the design of parallel architecture
- Evaluate the use of look-ahead techniques in parallel and pipelined IIR Digital filters.
- Develop an algorithm or architecture or circuit design for DSP applications

Question paper pattern:

- The question paper will have 10 full questions carrying equal marks.
- Each full question consists of 16 marks with a maximum of four sub questions.
- There will be 2 full questions from each module covering all the topics of the module
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Book:

Keshab K.Parthi, "VLSI Digital Signal Processing systems, Design and implementation ", Wiley 1999.

Reference Books:

1. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw-Hill,1994.

2. S.Y. Kung, H.J. White House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.

3. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994.

4. Lars Wanhammar, “DSP Integrated Circuits”, Academic Press Series in Engineering, 1st Edition.

PATTERN RECOGNITION and MACHINE LEARNING **[As per Choice Based Credit System (CBCS) scheme]** **SEMESTER – III**			
Course Code	**18ESP332**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**
Credits – 04			

Course objectives: The objective of the course is to discusses main and modern concepts for model selection and parameter estimation in recognition, decision making and statistical learning problems. Special emphasis will be given to regression, classification, regularization, feature selection and density estimation in supervised mode of learning.

Modules	**RBT Levels**
Module-1	
Introduction: Probability Theory, Model Selection, The Curse of Dimensionality, Decision Theory, Information Theory **Distributions:** Binary and Multinomial Variables, The Gaussian Distribution, The Exponential Family, Nonparametric Methods.**(Ch.: 1,2)**	**L1,L2**
Module-2	
Supervised Learning **Linear Regression Models:** Linear Basis Function Models, The Bias-Variance Decomposition, Bayesian Linear Regression, Bayesian Model Comparison **Classification&Linear Discriminant Analysis:** Discriminant Functions, Probabilistic Generative Models, Probabilistic Discriminative Mode**(Ch. :3,4)**	**L1,L2,L3**
Module-3	
Supervised Learning **Kernels:** Dual Representations, Constructing Kernels, Radial Basis Function Network, Gaussian Processes **Support Vector Machines:** Maximum Margin Classifiers, Relevance Vector Machines **Neural Networks:** Feed-forward Network, Network Training, Error Backpropagation**(Ch:5,6,7)**	**L1,L2,L3**
Module-4	
Unsupervised Learning: **Mixture Models:** K-means Clustering, Mixtures of Gaussians, Maximum likelihood,EM for Gaussian mixtures, Alternative View of EM. **Dimensionality Reduction:** Principal Component Analysis, Factor/Component Analysis, Probabilistic PCA, Kernel PCA, Nonlinear Latent Variable Models **(Ch.:9,12)**	**L1,L2,L3**
Module-5	

Probabilistic Graphical Models: Bayesian Networks, Conditional Independence, Markov Random Fields, Inference in Graphical Models, Markov Model, Hidden Markov Models**(Ch.:8,13)**	**L1,L2,L3**

Course Outcomes: At the end of this course, students will be able to

- Identify areas where Pattern Recognition and Machine Learning can offer a solution.
- Describe the strength and limitations of some techniques used in computational Machine Learning for classification, regression and density estimation problems.
- Describe and model data.
- Solve problems in Regression and Classification.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

1. Pattern Recognition and Machine Learning. Christopher Bishop. Springer, 2006

Internet of Things
[As per Choice Based Credit System (CBCS) scheme]
SEMESTER – III

Course Code	**18ECS333**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**04**	**SEE Marks**	**60**
Total Number of Lecture Hours	**50 (10 Hours per Module)**	**Exam Hours**	**03**

Credits – 04

Course objectives: This course will enable students to:

- Introduce concept of IOT and its applications in today's scenario.
- Understand IOT content generation and transport through networks
- Understand the devices employed for IOT data acquisition and communication access technologies
- Introduce some use cases of IOT

Module-1	**RBT**
What is IOT Genesis, Digitization, Impact, Connected Roadways, Buildings, Challenges **IOT Network Architecture and Design** Drivers behind new network Architectures, Comparing IOT Architectures, M2M architecture, IOT world forum standard, IOT Reference Model, Simplified IOT Architecture.	**L1, L2**
Module-2	
IOT Network Architecture and Design Core IOT Functional Stack, Layer1(Sensors and Actuators) , Layer 2(Communications Sublayer), Access network sublayer, Gateways and backhaul sublayer, Network transport sublayer, IOT Network management. Layer 3(Applications and Analytics) – Analytics vs Control, Data vs Network Analytics IOT Data Management and Compute Stack	**L2,L3**
Module-3	
Engineering IOT Networks Things in IOT – Sensors, Actuators, MEMS and smart objects. Sensor networks, WSN, Communication protocols for WSN Communications Criteria, Range Frequency bands, power consumption, Topology, Constrained Devices, Constrained Node Networks IOT Access Technologies, IEEE 802.15.4 Competitive Technologies – Overview only of IEEE 802.15.4g, 4e, IEEE 1901.2a Standard Alliances – LTE Cat0, Cat-M, NB-IOT	**L2,L3**
Module-4	

Engineering IOT Networks IP as IOT network layer, Key Advantages, Adoption, Optimization, Constrained Nodes, Constrained Networks, IP versions, Optimizing IP for IOT. Application Protocols for IOT – Transport Layer, Application Transport layer, Background only of SCADA, Generic web based protocols, IOT Application Layer Data and Analytics for IOT – Introduction, Structured and Unstructured data, IOT Data Analytics overview and Challenges.	**L3,L4**
Module-5	
IOT in Industry (Three Use cases) • IOT Strategy for Connected manufacturing, Architecture for Connected Factory • Utilities – Power utility, IT/OT divide, Grid blocks reference model, Reference Architecture, Primary substation grid block and automation. • Smart and Connected cities –Strategy, Smart city network Architecture, Street layer, city layer, Data center layer, services layer, Smart city security architecture, Smart street lighting.	**L3,L4**

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Course Outcomes: After studying this course, students will be able to:

- Understand the basic concepts IOT Architecture and devices employed.
- Analyze the sensor data generated and map it to IOT protocol stack for transport.
- Apply communications knowledge to facilitate transport of IOT data over various available communications media.
- Design a use case for a typical application in real life ranging from sensing devices to analyzing the data available on a server to perform tasks on the device.

Text Book:

Cisco, IOT Fundamentals – Networking Technologies, Protocols, Use Cases for IOT, Pearson Education; First edition (16 August 2017). ISBN-10: 9386873745, ISBN-13: 978-9386873743

Reference Books:

Arshdeep Bahga and Vijay Madisetti, 'Internet of Things – A Hands on Approach', Orient Blackswan Private Limited - New Delhi; First edition (2015), ISBN-10: 8173719543, ISBN-13: 978-8173719547